10/739701 Examiner: DINH, SON GAU: 2824
Inventor: MCPARTLAND , RICHARD Classification: 365/201.000
Status: 30 - DOCKETED NEW CASE - READY FOR EXAMINATION
Title: SEMICONDUCTOR MEMORY REPAIR METHODOLOGY USING QUASI-NON-VOLATILE MEMORY

Incoming tab report (6 items, not sorted)

Img	Status	Doc Code	Document Type	Receipt Date	Pages	Annotations
	7	TRNA	Transmittal letter	12/18/2003	2	
	7	SPEC	Specification	12/18/2003	15	
	7	CLM	Claims	12/18/2003	4	
	7	ABST	Abstract	12/18/2003	1	
	7	DRW	Drawings	12/18/2003	2	
	7	OATH	Oath or Declaration filed	12/18/2003	3	

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L1	1	(double adj high adj memory) and interface	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:46
L2	1408	interface and DDR	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:46
L3	788	2 and SDRAM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:47
L4	4	3 and (Dimm adj connector)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:49
L5	535	2 and module	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:49
L6	267	5 and (DDR adj SDRAM)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:50
L7	90	6 and connector	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:50
L8	84	7 and single	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:50
L9	72	8 and double	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/29 11:50